



December 12, 2003

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
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Subject: | Serial No. 10/664,262 09/17/03 |

Yong Meng Lee et al.

METHOD OF FORMING DOUBLE-GATED  
SILICON-ON-INSULATOR (SOI)  
TRANSISTORS WITH REDUCED GATE TO  
SOURCE-DRAIN OVERLAP CAPACITANCE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

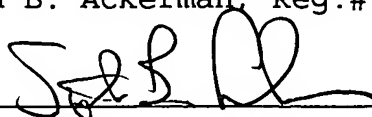
The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
mail in an envelope addressed to: Commissioner for Patents,  
P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 12/19/03

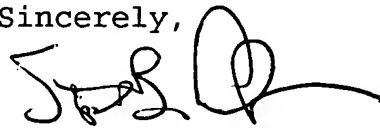
U.S. Patent 6,451,656 to Yu et al., "CMOS Inverter Configured From Double Gate MOSFET and Method of Fabricating Same," describes a double-gate transistor on semiconductor-on-insulator (SOI).

U.S. Patent 6,413,802 to Hu et al., "FinFET Transistor Structures Having a Double Gate Channel Extending Vertically From a Substrate and Methods of Manufacture," describes a double-gate FinFET on semiconductor-on-insulator (SOI).

U.S. Patent 6,365,465 to Chan et al., "Self-Aligned Double-Gate MOSFET by Selective Epitaxy and Silicon Wafer Bonding Techniques," describes a process for a double-gate MOSFET on semiconductor-on-insulator (SOI).

U.S. Patent 6,396,108 to Krivokapic et al., "Self-Aligned Double Gate Silicon-On-Insulator (SOI) Device," describes a process for a double-gate MOSFET on semiconductor-on-insulator (SOI).

Sincerely,

A handwritten signature in black ink, appearing to read 'S. B. Ackerman', with a large, stylized loop at the end.

Stephen B. Ackerman,  
Reg. No. 37761

Applicant Number

10/664, 262

Yang Meng Lee et al.

09/17/03

Group Art Unit

(Use several shouts if necessary)

DEC 22 2003

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## FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion, Pages, Etc.)


EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.